

Amendments to the Claims:

This listing of the claims will replace all prior versions and listings of the claims in the application:

1. (Currently amended) A power amplifier circuit for amplifying an input RF signal with respect to a specified RF output power, comprising
[[--]] an input terminal (2) for supplying the input RF signal to be amplified; [[,]]
[[--]] an output terminal for the RF signal with the output power specified; [[,]]
[[--]] an amplification path (3) formed between the input terminal (2) and the output terminal (7) having a power amplification circuit (4) for amplifying the RF signal; [[,]]
[[--]] a bypass (5) formed between the input terminal (2) and the output terminal (7) for the RF signal to bypass the amplification path (3); [[,]]
[[--]] a control terminal (6) for controlling the operation of the amplification path (3) and the bypass (5) such[[,]] that an RF signal is either passed through the amplification path (3) or the bypass (5); [[,]]
~~characterised by~~
[[--]] a variable gain amplifier circuit (15) for [[a]] pre-amplification of the input RF signal which is placed between the line from the input terminal (2) to the amplification path (3) and the bypass (5); [[,]] and
[[--]] a delay control means (16, 17, 18, 19) for controlling the variable gain amplifier (15), the amplification path (3), and the bypass (5); [[,]]

wherein the variable gain amplifier, the amplification path, and the bypass in a first state are operable to achieve the RF output power specified, and wherein the delay control means is operable to configure the variable gain amplifier, the amplification path, and the bypass in a second state that is an inverse of the first state.

~~whereby, before setting the operating conditions of the variable gain amplifier (15), the amplification path (3), and the bypass (5) in a state to achieve the RF output power specified, the delay control means (16, 17, 18, 19) is adapted to first set the respective operating conditions in the inverse state thereof.~~

2. (Currently amended) A power amplifier circuit according to claim 1, wherein a delay time period for which the delay control means configures the variable gain amplifier, the

amplification path, and the bypass in the second state characterised in that the delay time period for which the delay control means (16, 17, 18, 19) sets the operating conditions of the variable gain amplifier (15), the amplification path (3), and the bypass (5) in the inverse state thereof corresponds to half the a settling time (τ) for an RF output power change.

3. (Currently amended) A power amplifier circuit according to claim 1 ~~or 2~~,
wherein characterised in that the delay control means comprises:
a latch trigger circuit (16) for controlling the operation of the amplification path (3) and the bypass (5);
a sample-and-hold circuit (17) for controlling the gain factor of the variable gain amplifier circuit (15);
a digital multiplexer circuit (18) for selecting a control signal; and
a delay circuit (19) for delaying a control signal by the a delay time period.
4. (Currently amended) A power amplifier circuit according to claim 1, wherein the bypass comprises: anyone of the claims 1, 2 or 3, characterised by the bypass (5) comprising
a first matching circuit (8);
a second matching circuit (9); and
a first controllable switch (10) for controllably adapting configuring an the impedance of the bypass to control ~~either block or open it for a passage of an~~ the RF signal.
5. (Currently amended) A power amplifier circuit according to claim 1, wherein the amplification path comprises: anyone of the claims 1 to 4, characterised by the amplification path (3) comprising
a third matching circuit; (14) and
a controllable second switch (11) for controllably adapting adjusting an the impedance of the amplification path (3) to either amplify the an RF signal or block the passage ~~for of~~ the RF signal.
6. (Currently amended) A power amplifier circuit according to claim 1, wherein the control terminal is configured anyone of the claims 1 to 5, characterised by the control terminal

- (6) ~~being adapted~~ to provide control information to the delay control means ~~(16, 17, 18, 19)~~.
7. (Currently amended) A power amplifier circuit according to claim 1, wherein ~~anyone of the claims 3 to 6, characterised by~~ the variable gain amplifier circuit ~~(15) comprising~~ comprises a digital and/or analogue gain control.
8. (Currently amended) A power amplifier circuit according to claim 1, wherein ~~anyone of the claims 3 to 6, characterised in that~~ the input RF signal is a signal coded for use in an UMTS communication system.
9. (Currently amended) A mobile terminal for a wireless telecommunication system comprising with a power amplifier circuit ~~(1")~~ according to claim 1 ~~one of the claims 1 to~~ 8.
10. (Currently amended) A method for amplifying an input RF signal with respect to a specified RF output power, comprising: ~~the steps of~~
[[-]] supplying the input RF signal to be amplified; [[,]]
[[-]] outputting the RF signal with the output power specified; [[,]]
[[-]] amplifying the RF signal in an amplification path (3) formed between an input terminal (2) and an output terminal (7); [[,]]
[[-]] selectively bypassing the amplification path (3) using a bypass; [[,]]
[[-]] controlling ~~the~~ operation of the amplification path (3) and the bypass (5) such that an RF signal is either passed through the amplification path (3) or the bypass (5); [[,]]
~~characterised by~~
[[-]] pre-amplifying the input RF signal by a variable gain amplifier circuit (15) which is placed between the line from the input terminal (2) to the amplification path (3) and the bypass (5); [[, and]]
[[-]] controlling the variable gain amplifier (15), the amplification path (3), and the bypass (5) by a delay control means ~~(16, 17, 18, 19)~~; [[,]]
operating the delay control means to configure the variable gain amplifier, the amplification path, and the bypass in a first state that is an inverse of a second state; then

operating the variable gain amplifier, the amplification path, and the bypass in the second state to achieve the RF output power specified.

~~whereby, before setting the operating conditions of the variable gain amplifier (15), the amplification path (3), and the bypass (5) in a state to achieve the RF output power specified, the respective operating conditions are at first set in the inverse state thereof via the delay control means (16, 17, 18, 19).~~

11. (Currently amended) A method according to claim 10, wherein a delay time period for which the delay control means configures the variable gain amplifier, the amplification path, and the bypass in the first state characterised by the step of setting the operating conditions of the variable gain amplifier (15), the amplification path (3), and the bypass (5) by the delay control means (16, 17, 18, 19) in the inverse state thereof for a delay time period that corresponds to half the a settling time (τ) for an RF output power change.
12. (Currently amended) A method according to claim 10 ~~or 11~~, wherein operating the delay control means comprises:
~~characterised by the step of~~
controlling the operation of the amplification path (3) and the bypass (5) by a latch trigger circuit (16) integrated in the control means; [[,]]
controlling the gain factor of the variable gain amplifier circuit (15) by a sample-and-hold circuit (17); [[,]]
selecting a control signal by a digital multiplexer circuit (18); [[,]] and
delaying a control signal by the a delay time period by a delay circuit (19).
13. (Currently amended) A method according to claim 10, wherein selectively bypassing the amplification path comprises: anyone of claims 10, 11 or 12,
~~characterised by the step of~~
adjusting an controllably adapting the impedance of the bypass to control either block or open it for a passage of an RF signal by using a first matching circuit (8), a second matching circuit (9), and a first controllable switch (10) integrated in the bypass (5).

14. (Currently amended) A method according to ~~anyone of the claims 10 to 13~~, claim 10,
wherein amplifying the RF signal comprises:
~~characterised by the step of~~
adjusting an ~~controllably adapting the~~ impedance of the amplification path (3) to either
amplify an RF signal or block the passage ~~of~~ for the RF signal using ~~by~~ a third matching
circuit (14) and a controllable second switch (11) integrated in the amplification path (3).
15. (Currently amended) A method according to claim 10, wherein controlling operation of
the amplification path comprises: ~~anyone of the claims 10 to 14~~, ~~characterised by the step~~
~~of~~
configuring a ~~adapting the~~ control terminal (6) to provide control information to the
delay control means (16, 17, 18, 19).